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(54) **PHASE CHANGE MEMORY ELEMENT**

(71) Applicant: **HIGGS OPL. CAPITAL LLC**, Dover, DE (US)

(72) Inventors: **Frederick T. Chen**, Hsinchu (TW); **Ming-Jinn Tsai**, Hsinchu (TW)

(73) Assignee: **HIGGS OPL. CAPITAL LLC**, Dover, DE (US)

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(62) Division of application No. 14/062,793, filed on Oct. 24, 2013, now Pat. No. 8,884,260, which is a division of application No. 12/269,282, filed on Nov. 12, 2008, now Pat. No. 8,604,457.

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H01L 47/00	(2006.01)
H01L 27/24	(2006.01)
H01L 45/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 27/24*** (2013.01); ***H01L 45/06*** (2013.01); ***H01L 45/122*** (2013.01); ***H01L 45/124*** (2013.01); ***H01L 45/128*** (2013.01); ***H01L 45/1233*** (2013.01); ***H01L 45/1253*** (2013.01); ***H01L 45/14*** (2013.01); ***H01L 45/144*** (2013.01); ***H01L 45/1608*** (2013.01); ***H01L 45/1691*** (2013.01)

(58) **Field of Classification Search**

CPC . H01L 31/0324; H01L 39/2412; H01L 45/06; H01L 45/141; H01L 2924/0111; H01L 2924/055

USPC 257/2, 4

See application file for complete search history.

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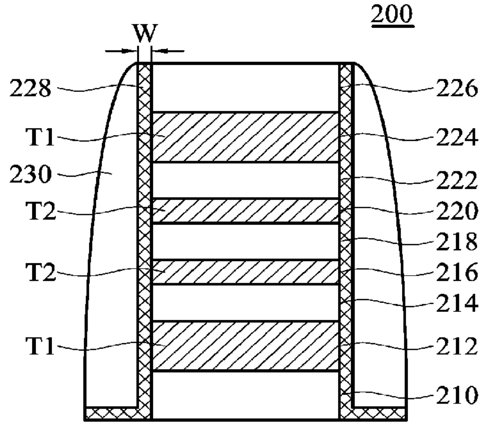
Primary Examiner — Hoai V Pham

(74) *Attorney, Agent, or Firm* — Schwabe Williamson & Wyatt

(57) **ABSTRACT**

A phase-change memory element with an electrically isolated conductor is provided. The phase-change memory element includes: a first electrode and a second electrode; a phase-change material layer electrically connected to the first electrode and the second electrode; and at least two electrically isolated conductors, disposed between the first electrode and the second electrode, directly contacting the phase-change material layers.

20 Claims, 8 Drawing Sheets



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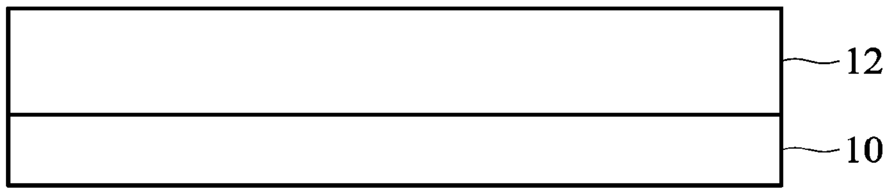

FIG. 1a

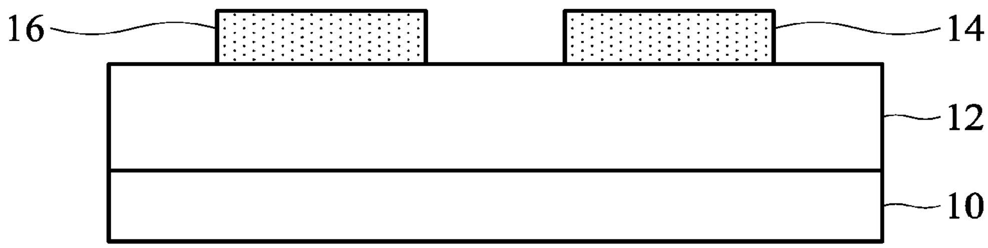

FIG. 1b

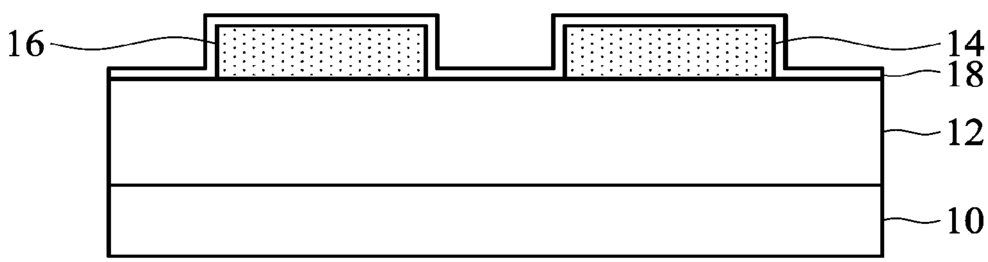

FIG. 1c

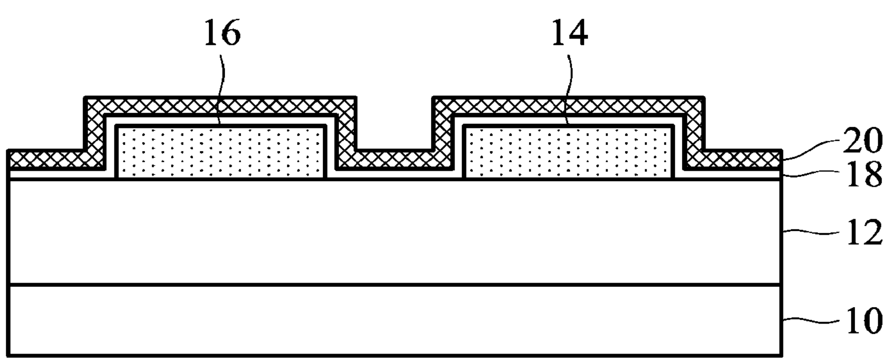

FIG. 1d

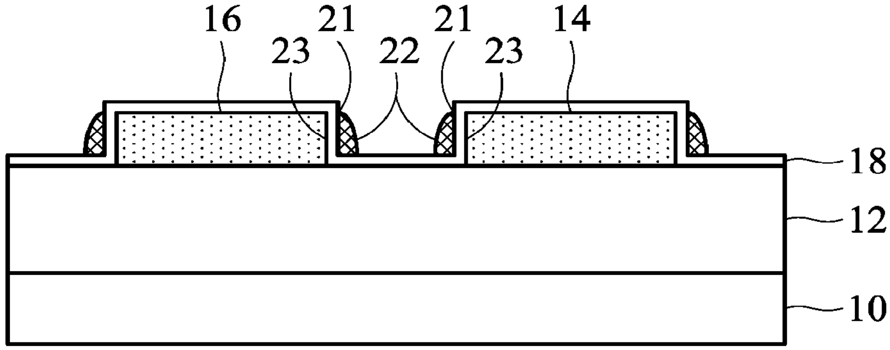

FIG. 1e

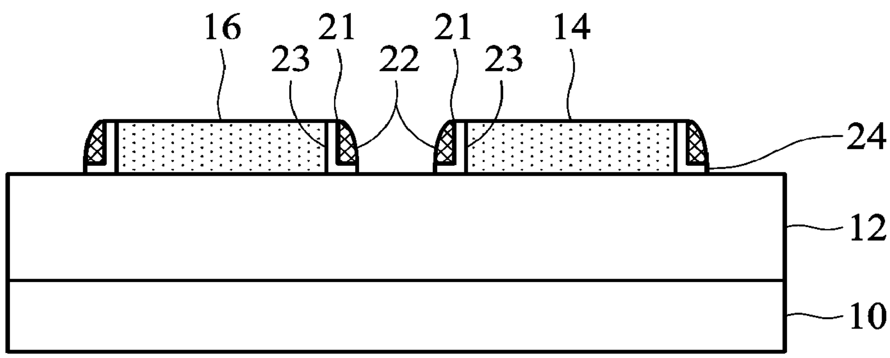

FIG. 1f

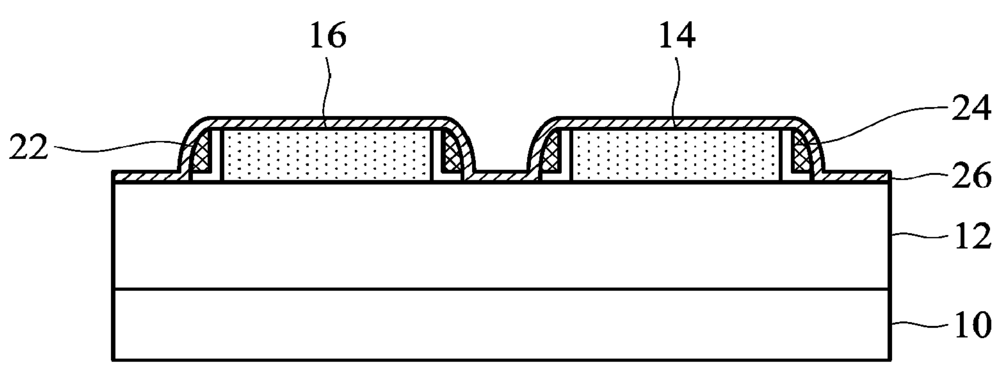

FIG. 1g

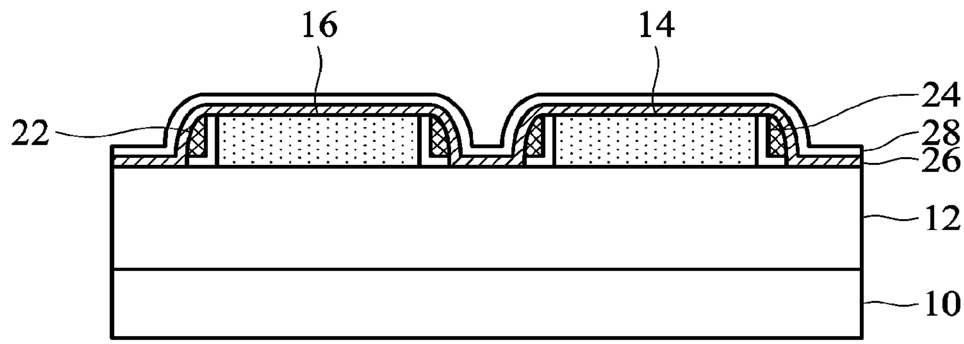

FIG. 1h

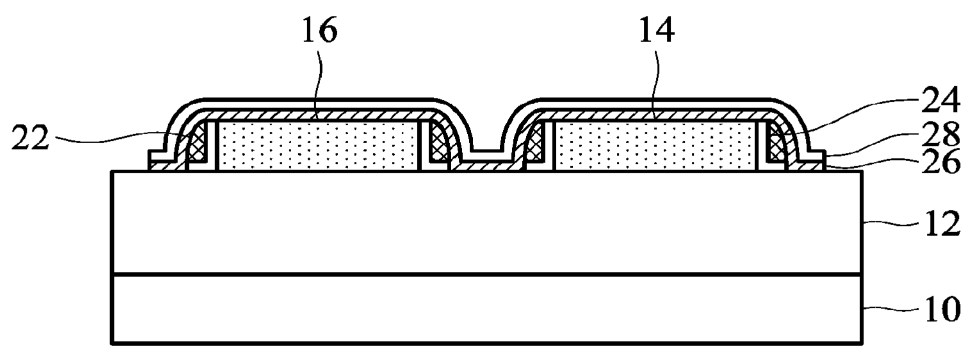

FIG. 1i

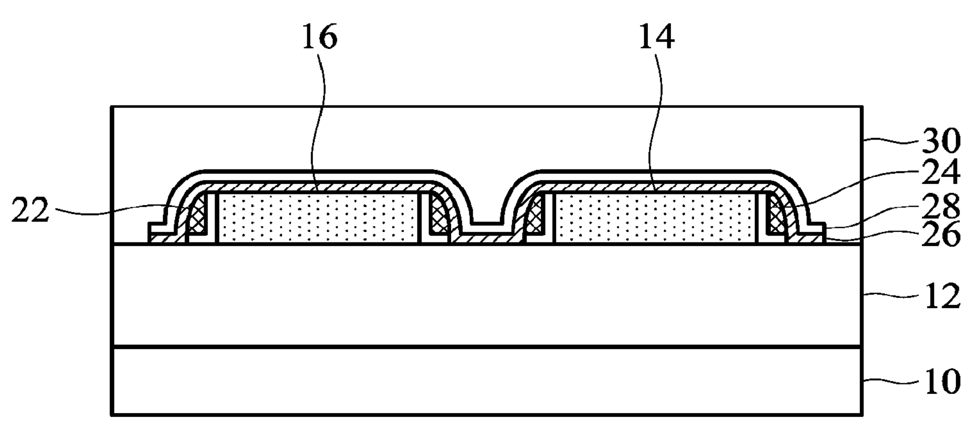

FIG. 1j

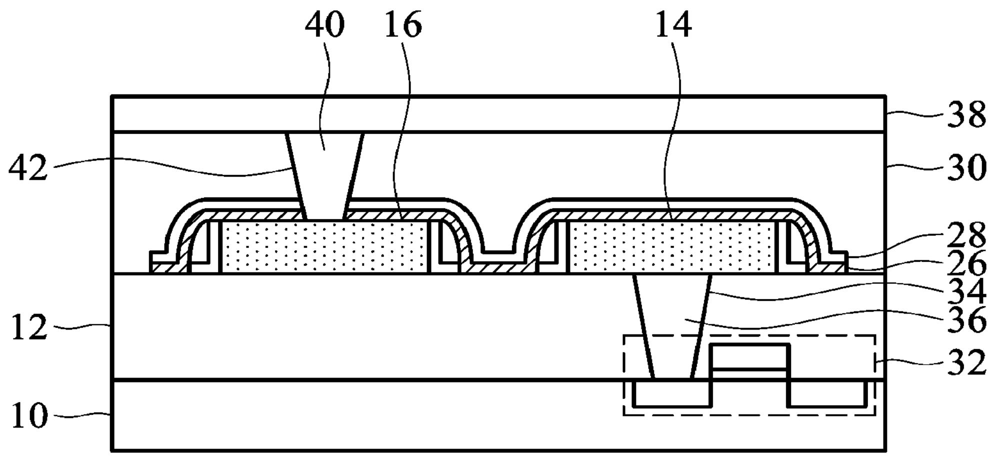

FIG. 2

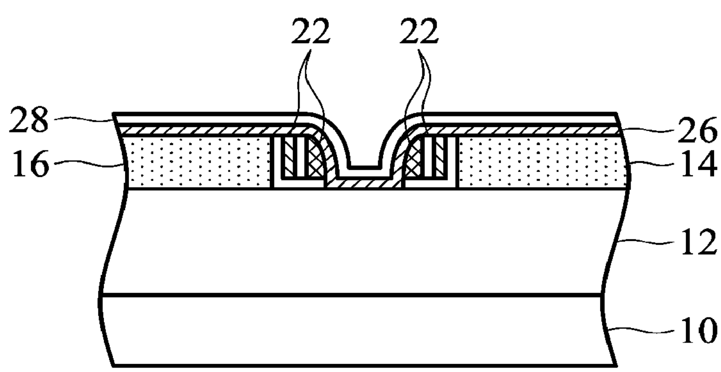

FIG. 3

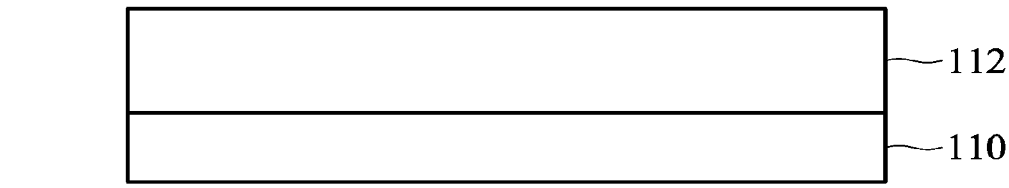

FIG. 4a

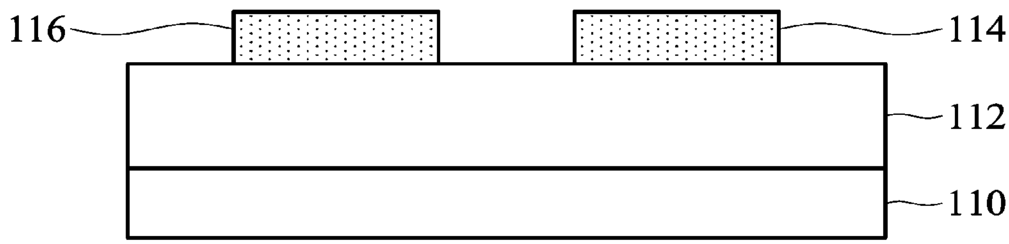

FIG. 4b

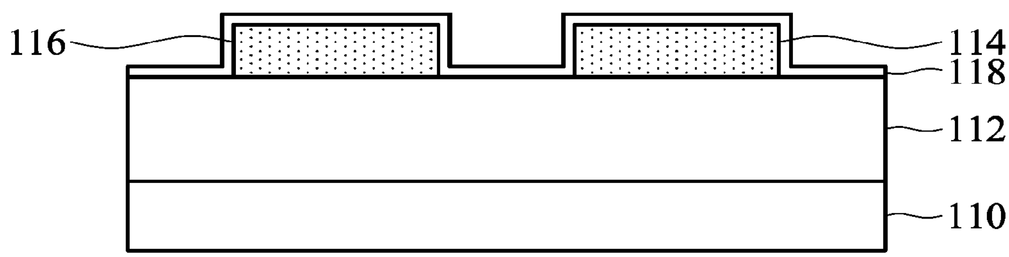

FIG. 4c

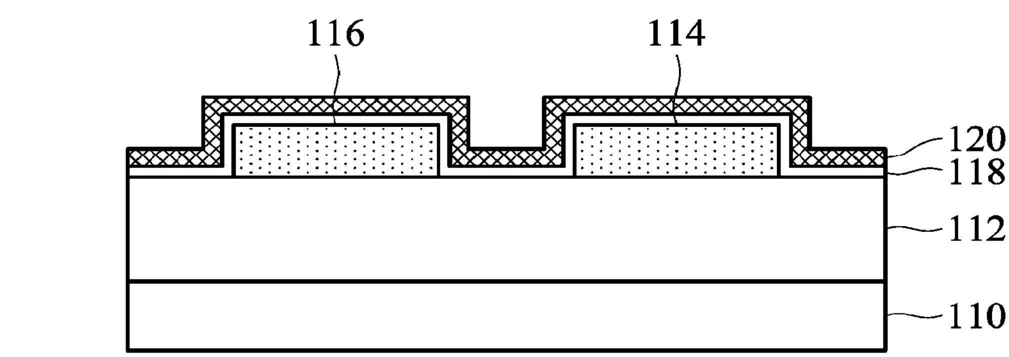

FIG. 4d

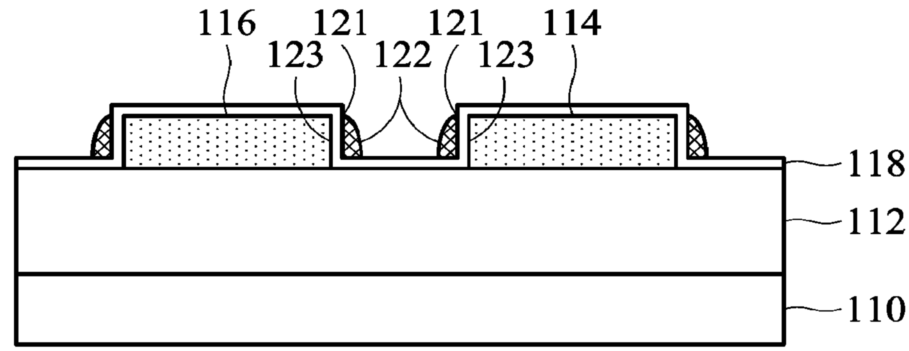

FIG. 4e

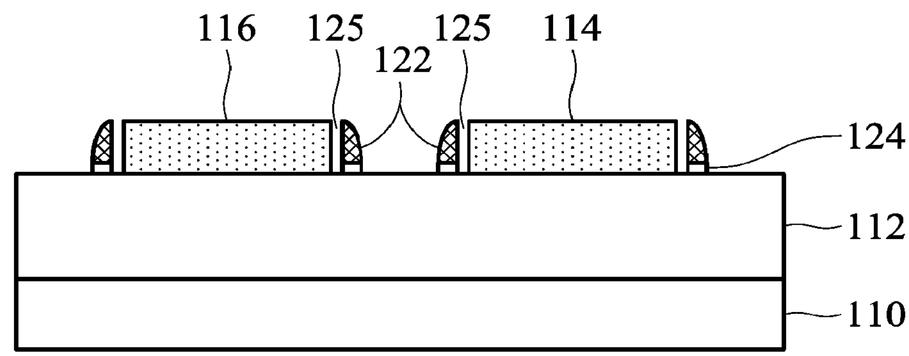

FIG. 4f

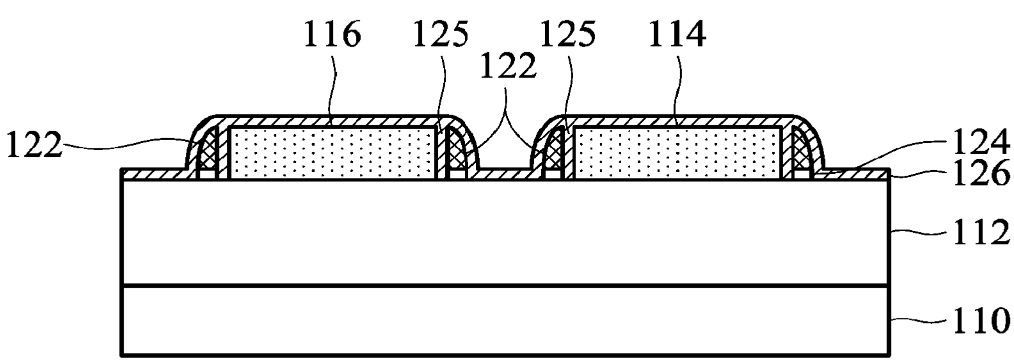

FIG. 4g

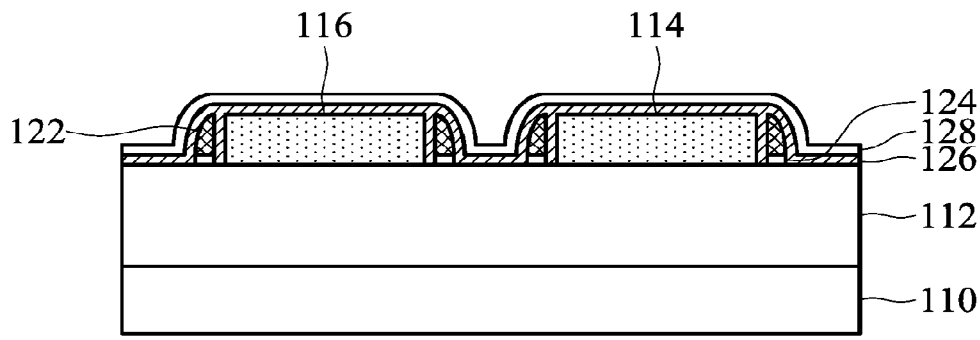

FIG. 4h

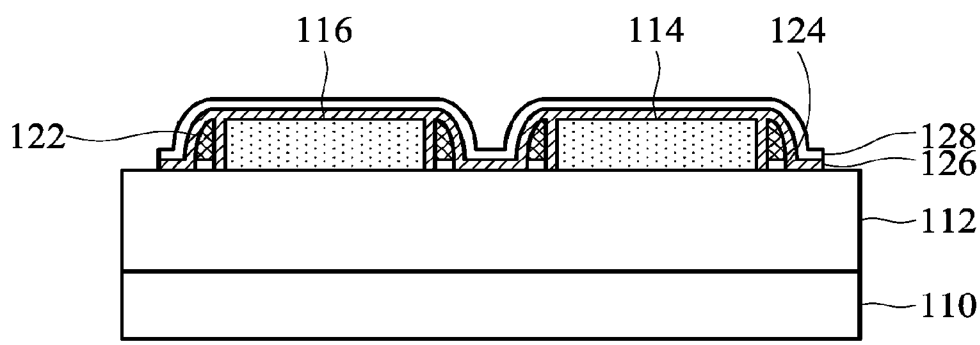

FIG. 4i

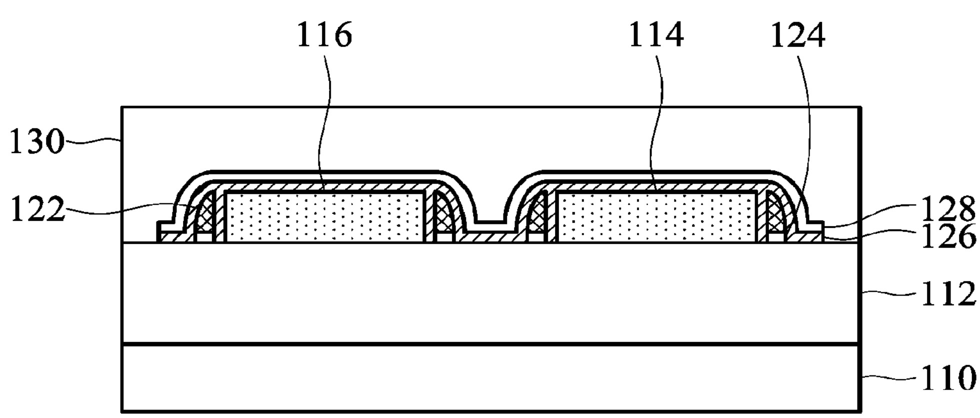

FIG. 4j

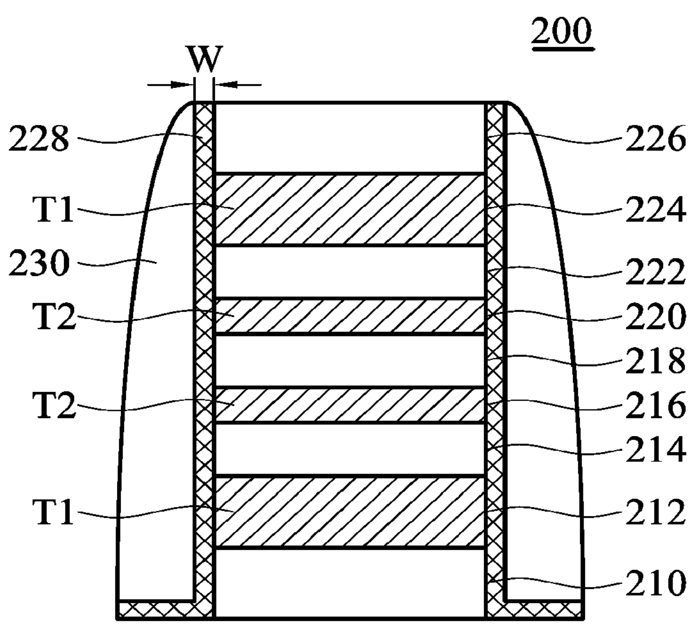

FIG. 5

PHASE CHANGE MEMORY ELEMENT

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of U.S. patent application Ser. No. 14/062,793, filed Oct. 24, 2013, which is a divisional of U.S. patent application Ser. No. 12/269,282, filed Nov. 12, 2008, the disclosures of which are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a memory element, and more particularly to a phase-change memory element.

2. Description of the Related Art

Phase-change memory technology requires high reliability, high speeds, low current, and low operating voltage, in order to function as a viable alternative to current memory technologies such as flash and DRAM. A phase-change memory cell must therefore provide low programming current, voltage operation, a smaller cell size, a fast phase transformation speed, and a low cost. These requirements are difficult to meet given the current state of the art.

The phase-change memory structures are predominantly self-heating, i.e. current flows through the phase-change material to produce the required heat. The top electrical contact of the phase-change memory is generally wider than the bottom electrical contact area. The structure may be a pore filled with phase-change material, or a block of phase-change material with a sublithographic bottom contact, and lithographically defined top electrode. The wider contact defines the maximum current required to write a bit to the cell. Variations in the bottom or top contact width due to lithography, etching or other processing stages result in variations of the required programming current.

Ideally, the phase-change memory will have a fixed cross-section area, such as a pillar or bridge. However these structures tend to require high voltages as the cross-section area and/or the length is reduced. An issue limiting further advancement is that the electrodes connecting to the structure, act as heat sinks.

Macronix (U.S. Pub. 20060284157 and U.S. Pub. 20060284158) disclosed a basic phase-change bridge structure. However, the electrode contacts are the only contacts to the bridge and heat significantly flows out through these contacts, thus making programming very inefficient.

U.S. Pat. No. 7,119,353 discloses a phase change memory element, including a substrate, a CMOS formed on the substrate, a dielectric layer, a metal plug, and a phase change memory cell. Particularly, the phase change memory cell includes a phase change material layer, and a pair of electrodes. The CMOS electrically connects to the electrode of the phase change memory cell via the metal plug. Accordingly, the active area (phase change area) can be determined by the thickness of the phase change material layer. The contact surface between the phase change material layer and the metal plug, however, is limited by the diameter of the metal plug, thereby making it unable to increase heating efficiency and reducing the programming current of the phase change memory cells.

Therefore, it is desirable to devise a phase-change memory cell structure that improves upon the aforementioned problems.

BRIEF SUMMARY OF THE INVENTION

An exemplary embodiment of a phase-change memory element includes: a first electrode and a second electrode; a phase-change material layer electrically connected to the first electrode and the second electrode; and at least two electrically isolated conductors, disposed between the first electrode and the second electrode, directly contacting the phase-change material layers.

An exemplary embodiment provides a method for forming a phase-change memory element, including providing a substrate; forming a dielectric layer on the substrate; forming a first electrode and a second electrode on the dielectric layer; forming at least two electrically isolated conductors on the dielectric layer, disposed between and separated from the first electrode and the second electrode; and forming a phase-change material layer electrically connected to the first electrode and the second electrode, directly contacting the phase-change material layer.

Another exemplary embodiment provides a method for forming phase-change memory element, including providing a substrate; forming a bottom electrode on the substrate; forming a first thermal insulator on the first electrode; forming a first electrically isolated conductor on the first thermal insulator; forming a dielectric layer on the first electrically isolated conductor; forming a second electrically isolated conductor on the dielectric layer; forming a second thermal insulator on the second electrically isolated conductor; forming a top electrode on the second thermal insulator; and forming a phase-change spacer to cover the side of above structure.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIGS. **1**a-**1**j are cross sections of a method for fabricating a phase-change memory element according to an embodiment of the invention.

FIG. **2** is a cross section of a device including the phase change memory element of the invention.

FIG. **3** is a cross section of a phase-change memory element according to another embodiment of the invention.

FIG. **4**a-**4**j are cross sections of a method for fabricating a phase-change memory element according to yet another embodiment of the invention.

FIG. **5** is a cross section of a phase-change memory element with electrically isolated conductors having a pillar structure according to embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The following description is of the best-contemplated mode of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

First, referring to FIG. **1**a, a substrate **10** with a dielectric layer **12** is provided. Particularly, the substrate **10** can be a substrate employed in a semiconductor process, such as silicon substrate. The substrate **10** can include a complementary metal oxide semiconductor (CMOS) circuit, an isolation structure, a diode, a transistor, or a capacitor (not shown). Suitable material for the dielectric layer **12** can include silicon dioxide.

Next, referring to FIG. **1**b, a pair of first and second electrodes **14** and **16** is formed on the dielectric layer **12** and separated from each other. Suitable material for the first and second electrodes **14** and **16**, for example, can be Al, W, Mo, Ti, TiN, TiAlN, TiW or TaN. The first electrode **14** may be electrically connected to lower layers of the substrate via a contact (not shown). The first and second electrodes **14** and **16** are formed by the same material and by the same process, and are coplanar.

Next, referring to FIG. **1***c*, a dielectric layers **18** is conformally formed on the substrate **10**, covering the dielectric layer **12** and the first and second electrodes **14** and **16**. The dielectric layer **18** can include silicon nitride, in order to prevent a subsequently formed metal layer from contacting the first and second electrodes **14** and **16**. The thickness of the dielectric layers **18** can be 10-50 nm.

Next, referring to FIG. **1***d*, a metal layer **20** is conformally formed on the dielectric layers **18**. The thickness of the metal layer **20** can be 10-50 nm. Suitable material of the metal layer includes Al, W, Mo, Ti, TiN, TiAlN, TiW or TaN.

Next, referring to FIG. **1***e*, an etching process (such as an anisotropic etching process) is subjected to the metal layer **20**, leaving a plurality of metal spacers **22** with a pointed top **21** sitting on the dielectric layer **18** adjacent to the side walls **23** of the first and second electrodes **14** and **16**.

Next, referring to FIG. **1***f*, another etching process (such as an anisotropic etching process) is subjected to the dielectric layers **18**, patterning the dielectric layers **18** leaving a patterned dielectric layers **24**.

Next, referring to FIG. **1***g*, a phase-change material layer **26** is conformally formed on the above substrate. The phase-change material layer **26** can include In, Ge, Sb, Te, Sn, Ga or combinations thereof, such as GeSbTe or InGeSbTe. It should be noted that there are two metal spacers **22** between the first and second electrodes **14** and **16** and the pointed top **21** and the side-walls of the two metal spacers **22** directly contact to the phase-change material layer **26**. Since the two metal spacers **22** are disconnected electrically from other components except for the phase-change material layer **26**, the two metal spacers **22** can serve as electrically isolated conductors of the phase-element. The thickness of the phase-change material layer **26** can be 0.5-10 nm.

Next, referring to FIG. **1***h*, a dielectric layer **28** is conformally formed on the phase-change material layer **26**. The dielectric layer **28** can include silicon nitride or the same material as the dielectric layer **18**.

Next, referring to FIG. **1***i*, the phase-change material layer **26** is patterned by lithography (such as one or two photomasks) to span the first and second electrodes **14** and **16** and have a bridge width comparable to a design rule. The phase-change bridge structure is therefore self-aligned to the electrodes. The dielectric layer **28** can include silicon nitride or the same material as the dielectric layer **18**.

Finally, referring to FIG. **1***j*, a dielectric layer **30** is formed on the above structure and planarized by a chemical mechanical planarization (CMP) process. The dielectric layer **30** can be silicon dioxide or the same material as the dielectric layer **12**. The dielectric layer **30**, dielectric layer **28** and the phase-change material layer **26** over the second electrode **16** may be patterned to form a via and the second electrode **16** can be electrically connected to a conductive layer via a contact (not shown).

According to an embodiment of the invention, referring to FIG. **2**, a device including the aforementioned phase change memory element is disclosed. The device includes a substrate having a transistor **32** formed thereon, wherein the transistor **32** is electrically connected to the first electrode **14** of the aforementioned phase-change memory element via a metal plug **34** with the contact hole **36**. The transistor **32** can further be electrically connected to a word line. Further, the device includes a bit line **38** electrically connected to the second electrode **16** of the aforementioned phase-change memory element via a metal plug **42** with the contact hole **40**.

In another embodiment of the invention, referring to FIG. **3**, the phase-change memory can have more than two metal spacers **22** between the first and second electrodes **14** and **16** to contact the phase-change material layer **26**, serving as electrically isolated conductors for multi-level operation.

Moreover, the invention also provides another phase-change memory element with the fabricating steps as below.

First, referring to FIG. **4***a*, a substrate **110** with a dielectric layer **112** is provided. Particularly, the substrate **110** can be a substrate employed in a semiconductor process, such as silicon substrate. The substrate **110** can include a complementary metal oxide semiconductor (CMOS) circuit, an isolation structure, a diode, a transistor, or a capacitor (not shown). Suitable material for the dielectric layer **112** can include silicon dioxide.

Next, referring to FIG. **4***b*, a pair of first and second electrodes **114** and **116** is formed on the dielectric layer **112** and is separated from each other. Suitable material for the first and second electrodes **114** and **116**, for example, can be Al, W, Mo, Ti, TiN, TiAlN, TiW or TaN. The first electrode **114** may be electrically connected to lower layers of the substrate via a contact (not shown). The first and second electrodes **114** and **116** are formed by the same material and by the same process, and are coplanar.

Next, referring to FIG. **4***c*, a dielectric layers **118** is conformally formed on the substrate **110**, covering the dielectric layer **112** and the first and second electrodes **114** and **116**. The dielectric layer **118** can include silicon nitride, in order to prevent a subsequently formed metal layer from contacting the first and second electrodes **114** and **116**. The thickness of the dielectric layers **118** can be 10-50 nm.

Next, referring to FIG. **4***d*, a metal layer **120** is conformally formed on the dielectric layers **118**. The thickness of the metal layer **120** can be 10-50 nm.

Next, referring to FIG. **4***e*, an etching process (such as an anisotropic etching process) is subjected to the metal layer **120**, leaving a plurality of metal spacers **122** with a pointed top **121** sitting on the dielectric layer **118** adjacent to the side walls **123** of the first and second electrodes **114** and **116**.

Next, referring to FIG. **4***f*, another etching process (such as an anisotropic etching process) is subjected to the dielectric layers **118**, patterning the dielectric layers **118** as the metal spacer as a mask, leaving a patterned dielectric layers **124**. Particularly, the patterned dielectric layers **124** and the adjacent electrode are separated by trenches **125**.

Next, referring to FIG. **4***g*, a phase-change material layer **126** is conformally formed on the above substrate and fills the trenches **125**. The phase-change material layer **126** can include In, Ge, Sb, Te, Sn, Ga or combinations thereof, such as GeSbTe or InGeSbTe. It should be noted that there are two metal spacers **122** between the first and second electrodes **114** and **116** and the pointed top **121** and the side-walls of the two metal spacers **122** directly contact two the phase-change material layer **126**. It should be noted that each metal spacer **122** and the electrode adjacent thereto are separated by the phase-change material layer **126** filled into the trenches. Since the two metal spacers **122** are disconnected electrically from other components except for the phase-change material layer **126**, the two metal spacers **122** can serve as electrically isolated conductors of the phase-element. The thickness of the phase-change material layer **126** can be 0.5-10 nm.

Next, referring to FIG. **4***h*, a dielectric layer **128** is conformally formed on the phase-change material layer **126**. The dielectric layer **128** can include silicon nitride or the same material as the dielectric layer **118**.

Next, referring to FIG. **4***i*, the phase-change material layer **126** is patterned by lithography (such as one or two photomask) to span the first and second electrodes **114** and **116** and have a bridge width comparable to a design rule. The phase-change bridge structure is therefore self-aligned to the electrodes. The dielectric layer **128** can include silicon nitride or the same material as the dielectric layer **118**.

Finally, referring to FIG. **4***j*, a dielectric layer **130** is formed on the above structure and planarized by a chemical mechanical planarization (CMP) process. The dielectric layer **130** can be silicon dioxide or the same material as the dielectric layer **112**. The dielectric layer **130**, dielectric layer **128** and the phase-change material layer **126** over the second electrode **116** may be patterned to form a via and the second electrode **116** can be electrically connected to a conductive layer of complementary metal oxide semiconductor (CMOS) circuit, an isolation structure, a diode, a transistor, or a capacitor (not shown) via a contact.

According to embodiments of the invention, a phase-change memory element **200** with electrically isolated conductors can have a pillar structure, as shown in FIG. **5**.

Referring to FIG. **5**, the phase-change memory element **200** includes, from bottom to top, a bottom electrode **210**, a first thermal insulator **212**, a first dielectric layer **214**, a first electrically isolated conductor **216**, a second dielectric layer **218**, a second electrically isolated conductor **220**, a third dielectric layer **222**, a second thermal insulator **224**, and a top electrode **226**. The phase-change memory element **200** further includes phase-change material spacers **228** covering all side walls of the above components, and a dielectric spacer **230** covering the phase-change material spacers. The bottom and top electrodes **210** and **226** can be independent and include Al, W, Mo, Ti, TiN, TiAlN, TiW or TaN. The first and second thermal insulators **212** and **224** can be a dielectric layer with low thermal conductivity or phase-change material. The dielectric layer **218** can be silicon dioxide. The first and second electrically isolated conductors **216** and **220** can be metal or phase-change material; phase-change material can include In, Ge, Sb, Te, Sn, Ga or combinations thereof, such as GeSbTe or InGeSbTe.

In the embodiment, the thermal insulator slows heating of the electrically isolated conductors and the phase-change area is confined to in-between the electrically isolated metal.

It should be noted that the width W of the phase-change material spacers **228** must be less than the thickness T**2** of the first and second electrically isolated conductors **216** and **220**. When the first and second thermal insulators **212** and **224** are phase-change material, the width W of the phase-change material spacers **228** must be less than the thickness T**1** of the first and second thermal insulators **212** and **224**. For example, the width W of the phase-change material spacers **228** can be 2-5 nm, the thickness T**2** of the first and second crystallization initiators **216** and **220** are 15 nm, and the thickness T**1** of the first and second thermal insulators **212** and **224** are 15 nm.

Accordingly, the phase-change memory element of the invention allows reduction of current and voltage and thermal non-uniformity in the programming region through manufacturing processes. Further, multi-bit capability is also possible. The bridge embodiment is not affected by the top contact critical dimension (CD) and bottom contact critical dimension (CD) variation issue.

While the invention has been described by way of example and in terms of preferred embodiment, it is to be understood that the invention is not limited thereto. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

The invention claimed is:

1. A phase-change memory, comprising:

a first electrode;

a second electrode;

an electrically-isolated conductor located between the first electrode and the second electrode; and

a phase-change material that contacts each of the first electrode, the second electrode, and the electrically-isolated conductor;

wherein the electrically-isolated conductor includes at least one of a thickness greater than a width of the phase-change material or a tapered end.

2. The phase-change memory of claim **1**, wherein the first electrode and the second electrode are coplanar.

3. The phase-change memory of claim **1**, wherein the second electrode is formed above the first electrode.

4. The phase-change memory of claim **1**, further comprising:

a transistor formed on the substrate, wherein a source or a drain of the transistor is electrically connected to the first electrode.

5. The phase-change memory of claim **4**, wherein at least a portion of the transistor is located below a surface of the substrate.

6. The phase-change memory of claim **5**, wherein the source or the drain is electrically connected to the first electrode via a metal plug formed in a hole on the surface of the substrate.

7. The phase-change memory of claim **1**, further comprising:

a diode formed on the substrate, wherein a terminal of the diode is electrically connected to the first electrode.

8. The phase-change memory of claim **1**, further comprising:

a complementary metal oxide semiconductor (CMOS) circuit formed on the substrate, wherein a terminal of the CMOS circuit is electrically connected to the first electrode.

9. The phase-change memory of claim **1**, wherein the electrically-isolated conductor comprises a plurality of electrically-isolated conductors.

10. The phase-change memory of claim **9**, wherein the electrically-isolated conductors of the plurality are separated by a dielectric layer.

11. The phase-change memory of claim **1**, wherein a memory cell corresponding to the electrically-isolated conductor comprises a multi-level memory cell.

12. The phase-change memory of claim **1**, wherein the phase change material comprises In, Ge, Sb, Te, Ga, Sn, or combinations thereof.

13. The phase-change memory of claim **1**, wherein the first electrode and the second electrode are independent and respectively comprise Al, W, Mo, Ti, TiN, TiAlN, TiW, or TaN.

14. The phase-change memory of claim **1**, wherein the electrically-isolated conductor comprises Al, W, Mo, Ti, TiN, TiAlN, TiW, or TaN.

15. The phase-change memory of claim **1**, wherein the first electrode and the second electrode are formed by the same process and made of the same material.

16. The phase-change memory of claim **1**, wherein the first electrode is electrically connected to an electrical element via a first metal plug.

17. The phase-change memory of claim **1**, wherein the second electrode is electrically connected to a bit line via a metal plug.

18. The phase-change memory of claim **1**, wherein the phase-change memory element comprises a pillar structure.

19. A phase-change memory, comprising:

a first electrode;

a second electrode;

an electrically-isolated conductor located between the first electrode and the second electrode; and

a phase-change material that contacts each of the first electrode, the second electrode, and the electrically-isolated conductor;

wherein the electrically-isolated conductor includes a thickness greater than a width of the phase-change material.

20. A phase-change memory, comprising:

a first electrode;

a second electrode;

an electrically-isolated conductor located between the first electrode and the second electrode; and

a phase-change material that contacts each of the first electrode, the second electrode, and the electrically-isolated conductor;

wherein the electrically-isolated conductor includes a pointed top.

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